

# FDMS86150

## N-Channel PowerTrench® MOSFET

100 V, 60 A, 4.85 mΩ

### Features

- Max  $r_{DS(on)}$  = 4.85 mΩ at  $V_{GS} = 10$  V,  $I_D = 16$  A
- Max  $r_{DS(on)}$  = 7.8 mΩ at  $V_{GS} = 6$  V,  $I_D = 13$  A
- Advanced Package and Silicon combination for low  $r_{DS(on)}$  and high efficiency
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

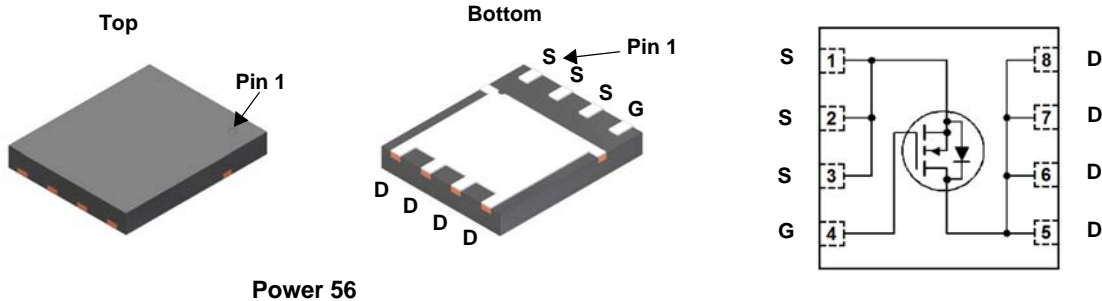


### General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced Power Trench® process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

### Applications

- Primary DC-DC MOSFET
- Secondary Synchronous Rectifier
- Load Switch



Power 56

### MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Conditions	Rated Value	Units
$V_{DS}$	Drain to Source Voltage		100	V
$V_{GS}$	Gate to Source Voltage		$\pm 20$	V
$I_D$	Drain Current	-Continuous $T_C = 25^\circ\text{C}$	60	A
		-Continuous $T_A = 25^\circ\text{C}$ (Note 1a)	16	
		-Pulsed	300	
$E_{AS}$	Single Pulse Avalanche Energy	(Note 3)	726	mJ
$P_D$	Power Dissipation	$T_C = 25^\circ\text{C}$	156	W
		$T_A = 25^\circ\text{C}$ (Note 1a)	2.7	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range		-55 to +150	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	Rated Value	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.8	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	45	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS86150	FDMS86150	Power 56	13"	12 mm	3000 units

## Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		72		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 80\text{ V}$ , $V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}$ , $V_{DS} = 0\text{ V}$			$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-10		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}$ , $I_D = 16\text{ A}$		3.9	4.85	m $\Omega$
		$V_{GS} = 6\text{ V}$ , $I_D = 13\text{ A}$		6	7.8	
		$V_{GS} = 10\text{ V}$ , $I_D = 16\text{ A}$ , $T_J = 125\text{ }^\circ\text{C}$		7.3	9.1	
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{ V}$ , $I_D = 16\text{ A}$		53		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 50\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$		3055	4065	pF
$C_{oss}$	Output Capacitance			696	930	pF
$C_{rss}$	Reverse Transfer Capacitance			29	50	pF
$R_g$	Gate Resistance		0.1	0.7	3.6	$\Omega$

### Switching Characteristics

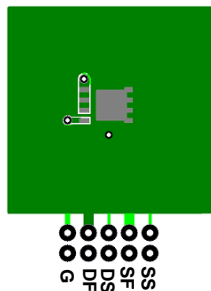
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\text{ V}$ , $I_D = 16\text{ A}$ , $V_{GS} = 10\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$		18	33	ns	
$t_r$	Rise Time			8.3	17	ns	
$t_{d(off)}$	Turn-Off Delay Time			28	45	ns	
$t_f$	Fall Time			6	12	ns	
$Q_g$	Total Gate Charge		$V_{GS} = 0\text{ V to }10\text{ V}$		44	62	nC
$Q_g$	Total Gate Charge		$V_{GS} = 0\text{ V to }5\text{ V}$	$V_{DD} = 50\text{ V}$ , $I_D = 16\text{ A}$	25	35	nC
$Q_{gs}$	Gate to Source Charge			12.9		nC	
$Q_{gd}$	Gate to Drain "Miller" Charge			9.2		nC	

### Drain-Source Diode Characteristics

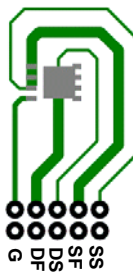
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = 2.1\text{ A}$ (Note 2)		0.69	1.2	V
		$V_{GS} = 0\text{ V}$ , $I_S = 16\text{ A}$ (Note 2)		0.78	1.3	
$t_{rr}$	Reverse Recovery Time	$I_F = 16\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		69	110	ns
$Q_{rr}$	Reverse Recovery Charge			94	150	nC

#### Notes:

- $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a. 45  $^\circ\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.

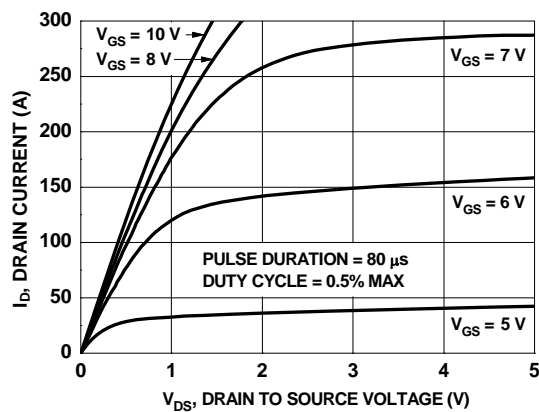


b. 115  $^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper.

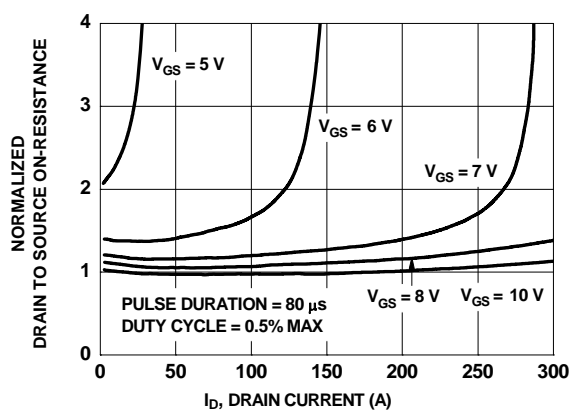
- Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0%.

- $E_{AS}$  of 726 mJ is based on starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 3\text{ mH}$ ,  $I_{AS} = 22\text{ A}$ ,  $V_{DD} = 100\text{ V}$ ,  $V_{GS} = 10\text{ V}$ , 100% test at  $L = 0.1\text{ mH}$ ,  $I_{AS} = 69\text{ A}$ .

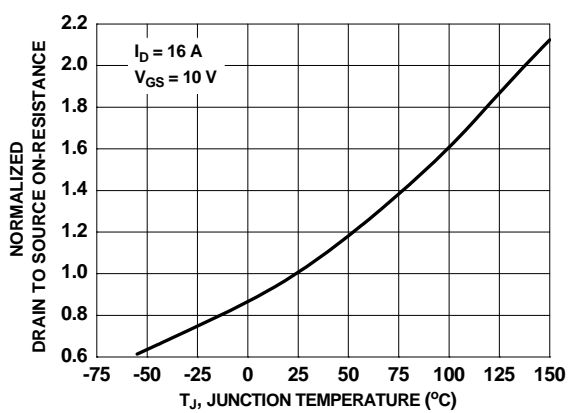
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



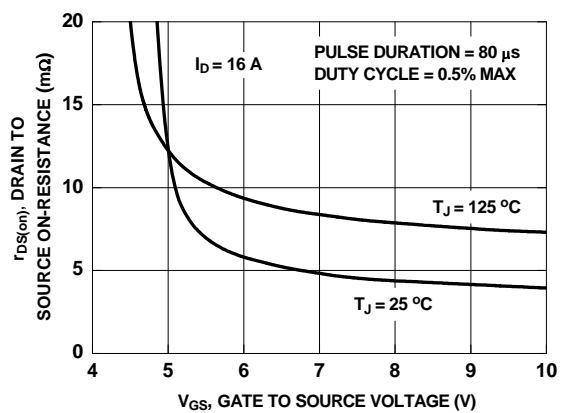
**Figure 1. On Region Characteristics**



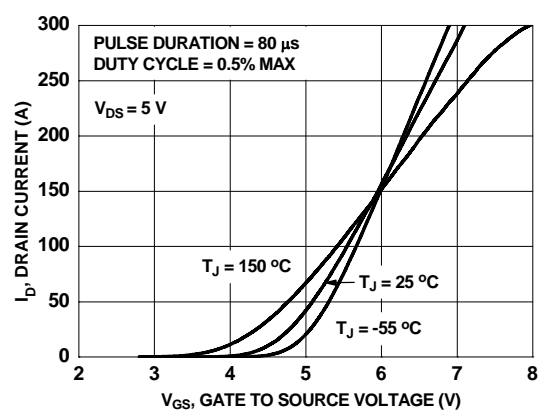
**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**



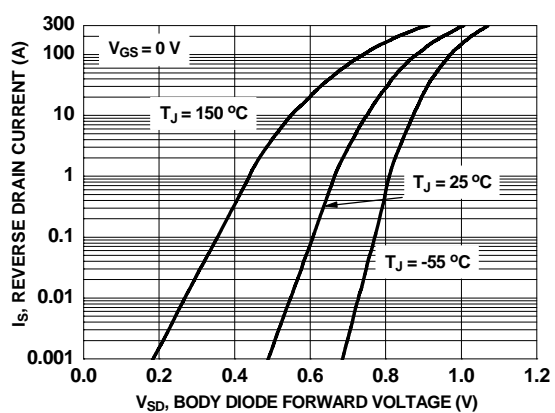
**Figure 3. Normalized On Resistance vs Junction Temperature**



**Figure 4. On-Resistance vs Gate to Source Voltage**

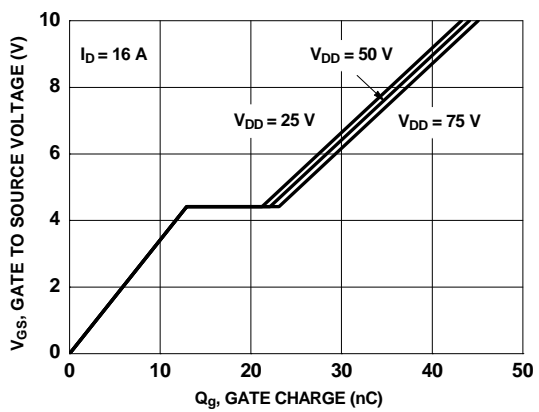


**Figure 5. Transfer Characteristics**

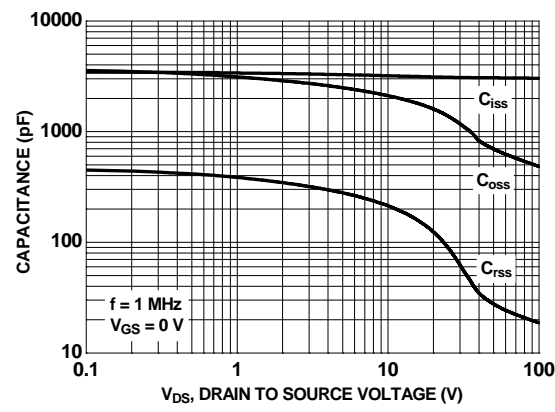


**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

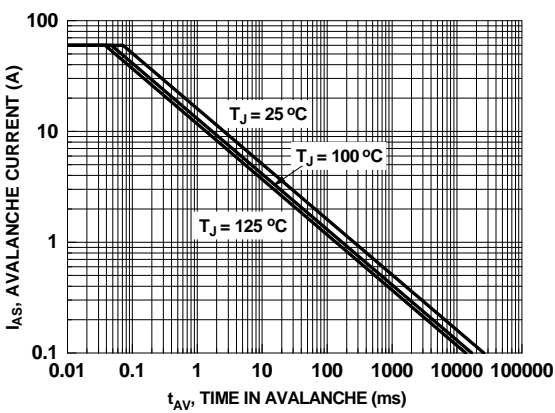
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



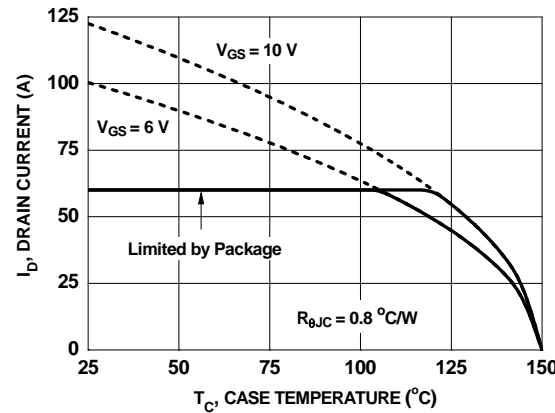
**Figure 7. Gate Charge Characteristics**



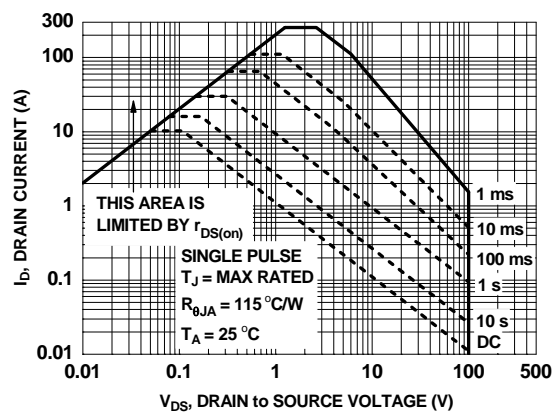
**Figure 8. Capacitance vs Drain to Source Voltage**



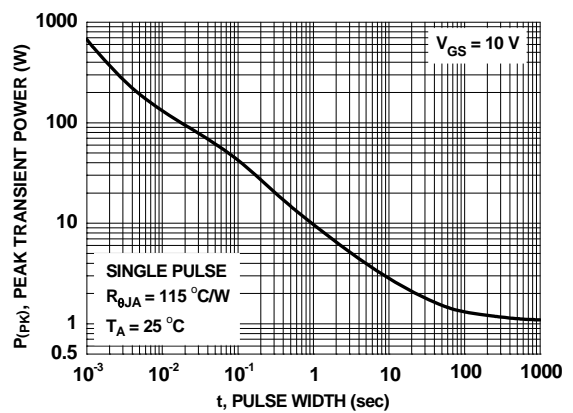
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Case Temperature**

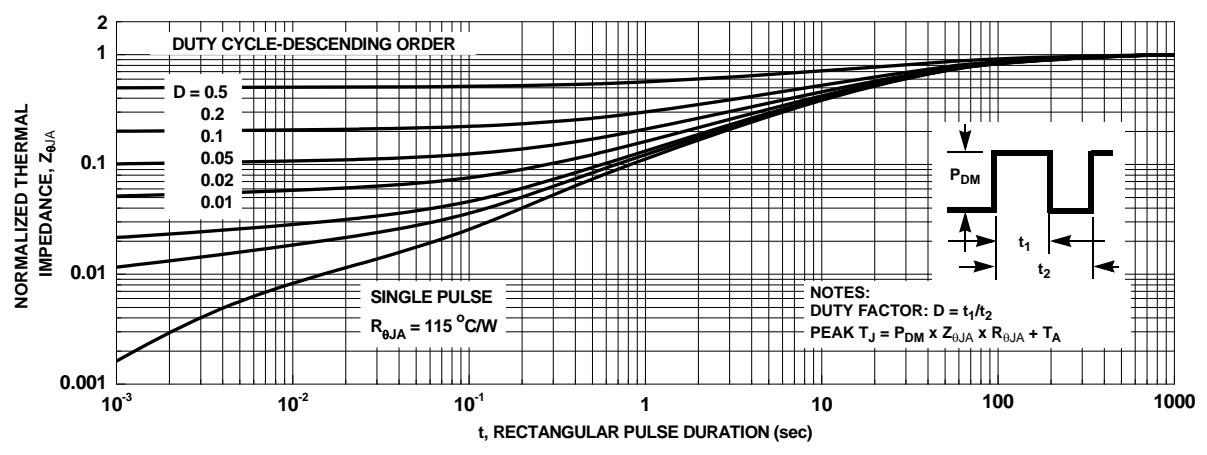


**Figure 11. Forward Bias Safe Operating Area**



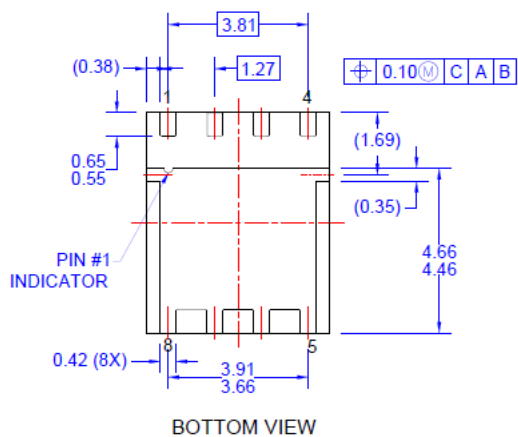
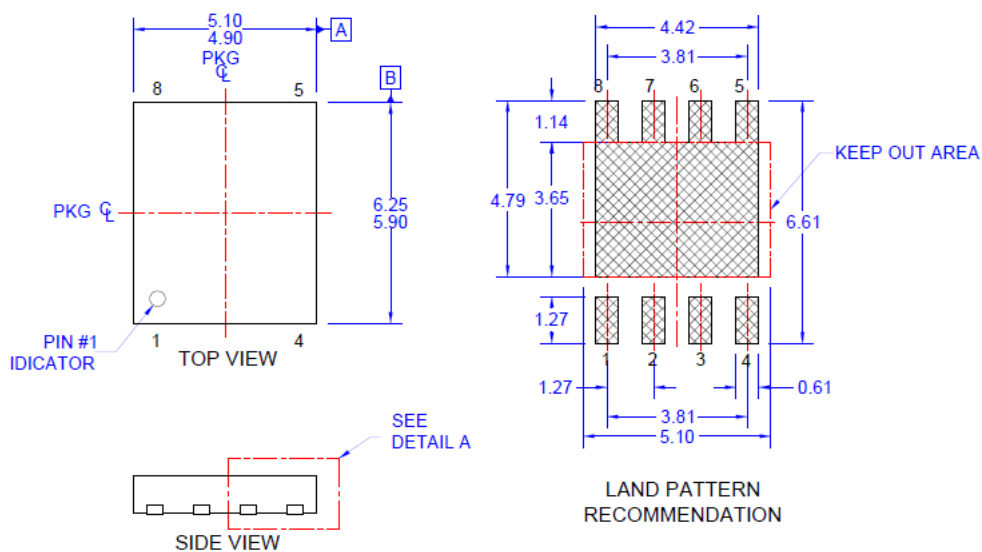
**Figure 12. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

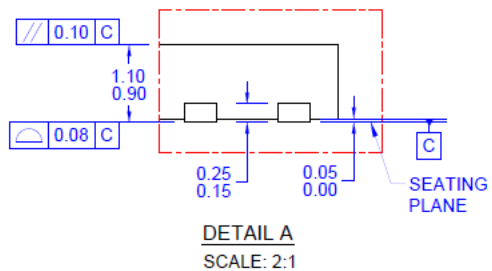


**Figure 13. Junction-to-Ambient Transient Thermal Response Curve**

## Dimensional Outline and Pad Layout








- NOTES: UNLESS OTHERWISE SPECIFIED
- A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA.
  - B) ALL DIMENSIONS ARE IN MILLIMETERS.
  - C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
  - D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
  - E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.
  - F) DRAWING FILE NAME: PQFN08JREV1.





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| AX-CAP™*  | Global Power Resource <sup>SM</sup>   | Programmable Active Droop™  | franchise   |
| BitSiC®   | Green Bridge™   | QFET®   | TinyBoost™  |
| Build it Now™   | Green FPS™  | QS™   | TinyBuck™   |
| CorePLUS™   | Green FPS™ e-Series™  | Quiet Series™   | TinyCalc™   |
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| FlashWriter®*   |  |  |   |
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Datasheet Identification	Product Status	Definition
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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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